SPACER-LESS TRANSISTOR INTEGRATION SCHEME FOR HIGH-K GATE DIELECTRICS AND SMALL GATE-TO-GATE SPACES APPLICABLE TO SI, SIGE AND STRAINED SILICON SCHEMES

ABSTRACT OF THE DISCLOSURE

A transistor integration process provides a damascene method for the formation of gate electrodes and gate dielectric layers. An interlayer-dielectric film is deposited prior to the gate electrode formation to avoid the demanding gap fill requirements presented by adjacent gates. A trench is formed in the interlayer-dielectric film followed by the deposition of the gate material in the trench. This process avoids the potential for damage to high-k gate dielectric layers caused by high thermal cycles and also reduces or eliminates the problematic formation of voids in the dielectric layers filling the gaps between adjacent gates.